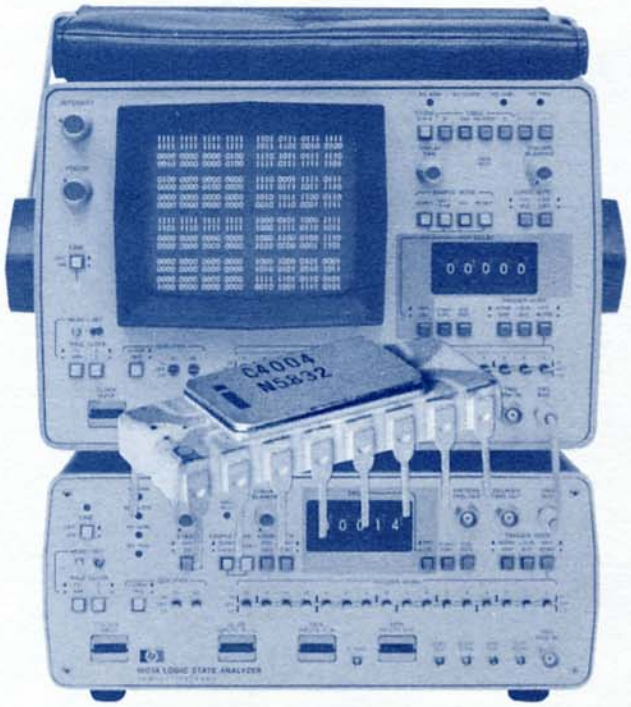
APPLICATION NOTE 167-15
DATA DOMAIN MEASUREMENT SERIES

Functional analysis of Intel 4004 microprocessor systems.



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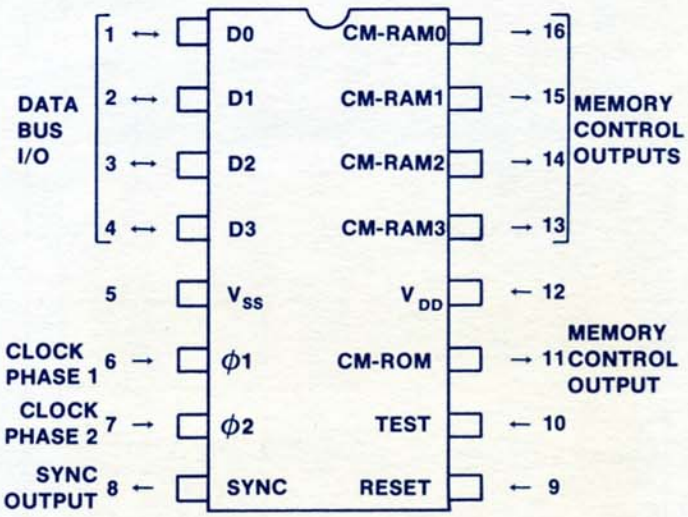
1. INTRODUCTION

This application note is designed to assist the 4004 Microprocessor family user in the real time analysis of his system—in both design and troubleshooting environments. The note demonstrates real time analysis of program flow, triggering on specific data events, as well as paging techniques.

The 4004 microprocessor, which is the heart of the 4004 microcomputer family, is fabricated with P-channel silicon gate MOS technology and operates from +5 volt and —10 volt power supplies. The 4004 features a 4-bit parallel CPU with 46 instructions. The 4004 can directly address 4k 8-bit instruction words of program memory and 5120 bits of data storage RAM. Up to 16 4-bit input ports and 16 4-bit output ports can also be directly addressed. Sixteen index registers are provided internal to the microprocessor for temporary data storage. The 4004 Microprocessor operates at clock rates to approximately 750 kHz.

2. PIN ASSIGNMENTS



SUMMARY OF DATA AND CONTROL LINES

D0-D3 Bidirectional data bus handling all address and data communication between the microprocessor and RAM and ROM chips.

ϕ1-ϕ2 Non-overlapping clock signals that determine microprocessor timing.

SYNC Synchronization signal indicating beginning of instruction cycle to ROM and RAM chips.

RESET A "1" level applied to RESET clears all flag and status flip-flops and forces the program counter to 0. RESET must be applied for 64 clock cycles (8 machine cycles) to completely clear all address and index registers.

TEST Input. The logic state of TEST can be examined with JCN instruction.

CM-ROM Line enables a ROM bank and I/O devices that are attached to the CM-ROM line.

CM-RAM0 thru CM-RAM3 Lines function as bank select signals for the RAM chips in the system.

3. PROBE CONNECTIONS

NOTE:
The 4004 Microprocessor does not provide a unique clock for the Logic State Analyzer at the proper time (end of A3 state) in the instruction cycle. The CM-ROM line is always true at A3 and can be used as a clock signal. However, CM-ROM also occurs at states M2 or X2 during the execution of some instructions. This would result in invalid data being displayed by the Analyzer. By constructing the circuit shown in figure 1, you can ensure a correct state display.

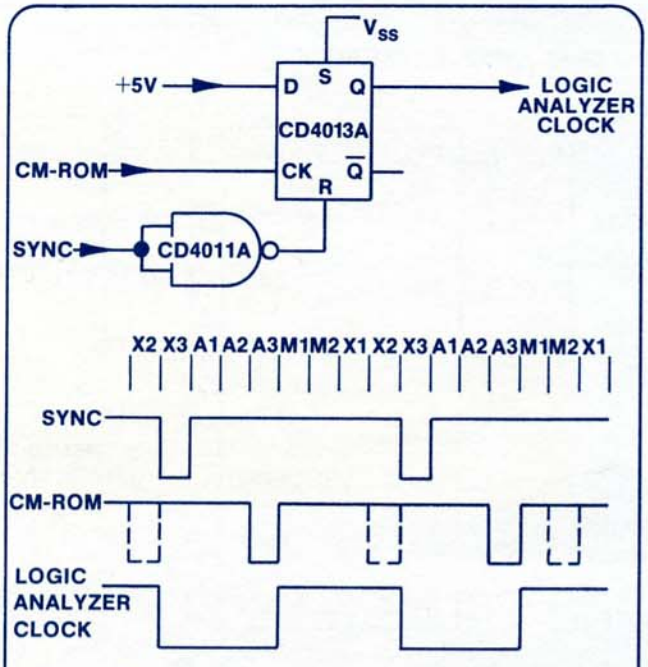
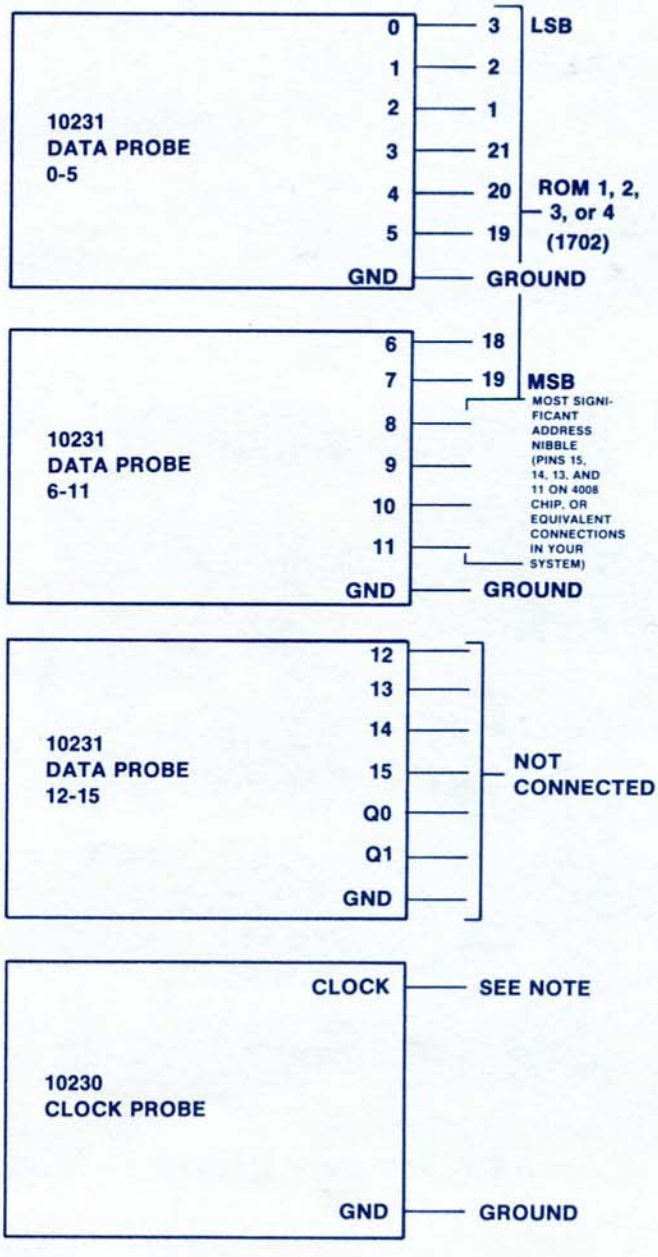


Figure 1. Circuit for Deriving a clock for the 1600A from 4004 Sync and CM-ROM signals.

If the portion of program you wish to examine is completely contained on one ROM, the chip select line (CS) for that ROM can be used as a clock.

A system that will not "come up" can frequently be debugged by monitoring address flow alone. The 4004 CPU chip has a 4-bit data bus, on which the 12-bit address is multiplexed during A1, A2, and A3 states of the 4004 machine cycle. In order to view the demultiplexed 12-bit address on a 1600A, the 4004 system must use 4008/4009 Standard Memory and I/O Interface Set, the 4289 Standard Memory Interface, or similar logic circuits that provide a demultiplexed address bus. If your system uses memory chips that internally decode the multiplexed address, such as the 4001 ROM, monitor the microprocessor data bus as described in Sections 9 and 10 of this application note.

The following probe connections provide a display of the activity on the address lines.



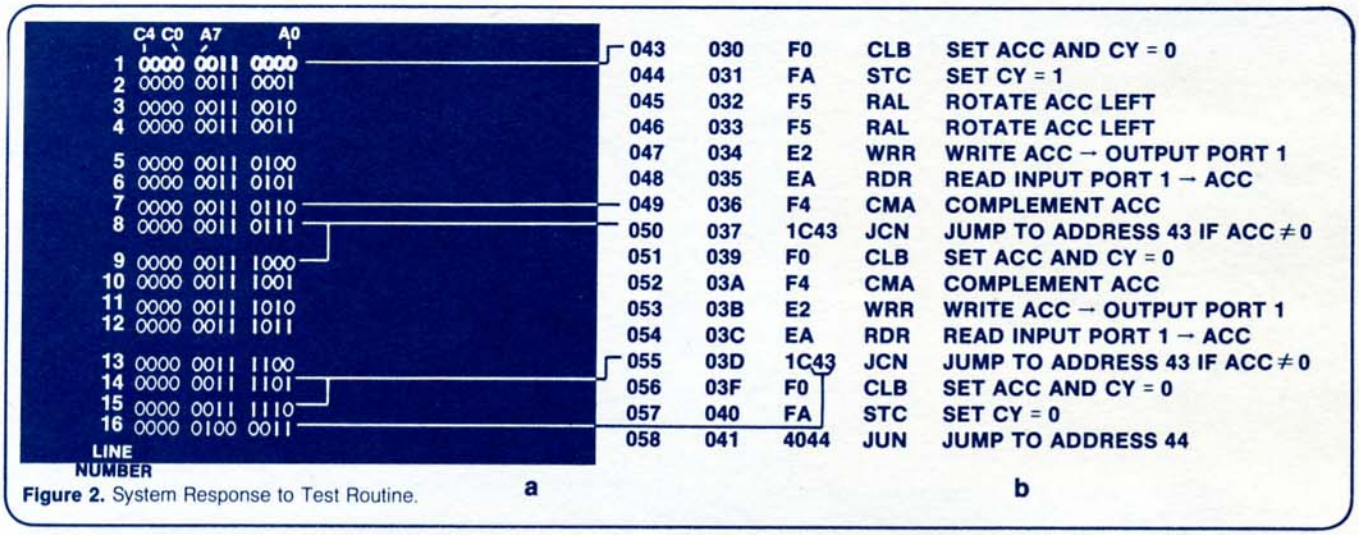


Figure 2. System Response to Test Routine.

4. SETTING THE CONTROLS

Turn power on and set Logic State Analyzer controls as follows:

Display Mode ..... Table A
Sample Mode [1] ..... SGL
Start Display ..... ON
Trigger Mode
NORM/ARM ..... NORM
LOCAL/BUS ..... LOCAL
OFF/WORD ..... WORD
Threshold [2] ..... VAR, adjust to 3.7 V
Logic ..... POS
Clock ..... ⌐
All Other Pushbuttons ..... Out Position
Display Time ..... ccw
Qualifiers Q1, Q0 ..... OFF
Trigger Word Switches ..... set to address at which you wish to trigger
Column Blanking ... after display is on screen, adjust blanking to display 12 columns of data

[1]SGL is selected for viewing single-shot events. Press RESET and start your system. The first time the system passes through the trigger point the display will be generated and stored. For programs that are looping or cycling through the selected address, select REPET sample mode.

[2]For TTL compatible systems, set threshold to TTL.

5. DISPLAY INTERPRETATION

In this illustration, a segment of a chip tester program for Quad NAND gates is examined. Proper operation is confirmed by a comparison between real time state analysis, figure 2a, and the 4004 cross assembler program listing output, figure 2b.

The chip tester routine performs the following events:

1. Sets up bit patterns in the accumulator.
2. Outputs the accumulator contents to the NAND gates (connected to I/O Port 1).
3. Reads the gate outputs.
4. Tests on the gate outputs and indicates whether chip is good or bad.

Consider the program listing, figure 2b. The instructions located in addresses 030 through 033 load the bit pattern 0010 into the accumulator. The next instruction (WRR), in location 034, writes the accumulator contents to output port 1. The next two instructions (address locations 035 and 036) read the gate outputs present at input port 1 into the accumulator and complement the accumulator. Examination of lines 1 through 7 of the state display photograph, figure 2a, shows that these instructions have been executed in the proper sequence.

The instruction starting at address 037 is a conditional jump which is a two-word instruction (lines 8 and 9 of the state display). If the chip passed the test (accumulator contains all zeros), the program continues the test routine. If the chip failed the test, the program jumps to an output routine. Examination of line 10 of the state display, address 039, reveals that the chip passed the test. The program then outputs another bit pattern (1111) to the chip under test and reads the input port. This is shown by lines 10 through 13 of the state display.

Lines 14 and 15 of the state display are the addresses of the two words of another JCN instruction. Line 16 of the state display is the address 043, showing that the chip failed the last test, causing the program to jump to the output routine.

6. THE MAP

If a tabular display is not presented in Section 5, it means the system did not access the selected address and the No Trigger light will be on. To find where the system is residing in the program switch to "map" (figure 3). Using the Trigger Word switches move the cursor (circle in photo) to encircle one of the dots on screen. Switch to Expand and make the final positioning of the cursor—the No Trigger light will now go out and switching back to Table A displays the 16 addresses around that point.

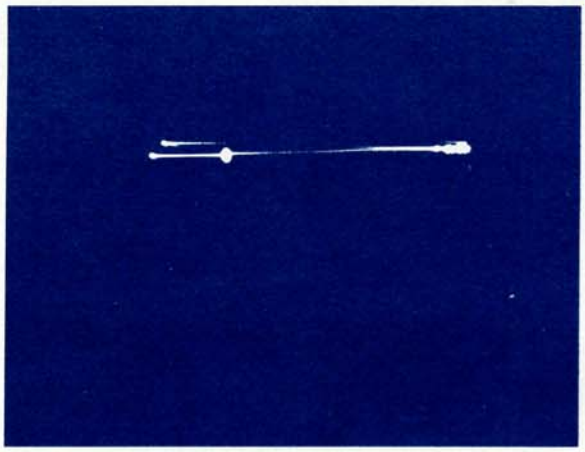


Figure 3. Map Display Shows Entire System Activity.

7. VIEWING ADDRESS, DATA, AND CONTROLS

When program deviations are found, the reason may be as simple as a program error or as complicated as a hardware failure on the data bus or command lines. Additional input channels now become very desirable.

By combining the 1600A and 1607A the display and trigger capability can be expanded to 32 bits wide, allowing the 12-bit address, 8-bit data word and up to 12 other active control signals to be viewed simultaneously. The hookup is easy:

1. Connect data cable between rear panel connectors.

2. Connect trigger bus cable between front panel bus connectors.

3. Set 1600A controls as described in Section 4 with the following exception: set display mode to Table A & B.

4. Set 1607A controls as follows:

Sample Mode	SINGLE
Start Display	ON
Trigger Mode	
NORM/ARM	NORM
LOCAL/BUS	BUS
OFF/WORD	OFF
Threshold, Logic, and Clock	same as 1600A
All Other Pushbuttons	Out Position
Qualifiers Q1, Q0	OFF

5. Connect data and clock inputs for 1607A as follows:
   a. Connect 1607A data inputs 0 through 7 to the demultiplexed data bus (ROM output) starting with LSB connected to 1607A data input 0.
   b. Connect 1607A clock input to signal used to clock 1600A.
   c. Connect grounds to appropriate points.
6. After a display is on screen, set the 1607A blanking to display eight columns.

8. DISPLAY INTERPRETATION OF ADDRESS AND DATA LINES

By displaying both address and data, it is now possible to confirm exact system operation with respect to the test routine. Looking at line 1 of the state display photograph, figure 4a, observe that the data corresponding to address 030 is F0, the 8-bit code for the CLB instruction. Looking at line 2, we see that the displayed data word agrees with the operation code for the STC instruction given in the program listing. In this manner, subsequent lines of the state display can be

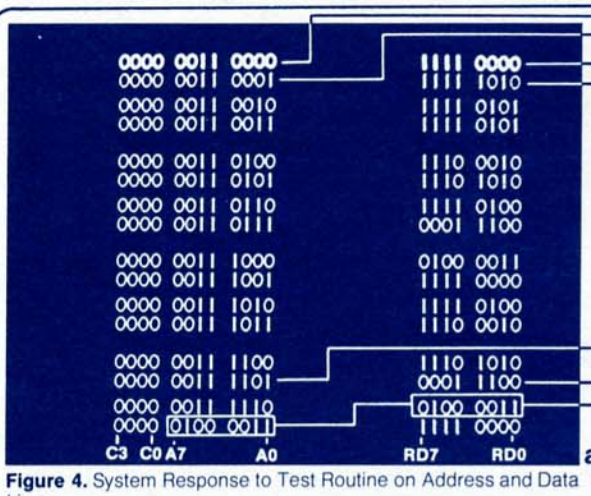


Figure 4. System Response to Test Routine on Address and Data Lines.

examined to show exact program operation. Note that line 14 of the state display corresponds to the first word of the JCN instruction at address 03D. The data in line 15 corresponds to the second word (0100 0011) of the JCN instruction, the address that program control is transferred to if the jump condition is true. Examination of line 16 reveals that the program did jump to the specified address.

9. VIEWING THE MULTIPLEXED DATA BUS

In the preceding examples, the demultiplexed address and data lines have been observed on the ROM address and data lines. However, when a hardware failure occurs, it may be very useful to directly observe activity on the multiplexed microprocessor data bus. In the following example, we shall observe data being demultiplexed into a 12-bit address for driving a ROM. Then we shall watch the ROM output being multiplexed back onto the bus.

Set up the 1600A and 1607A to obtain the display as follows:

1. Connect 1600A data, qualifier, and clock inputs as follows:
   a. 1600A data inputs 0 through 7 to RD0 through RD7 on the ROM in order.
   b. 1600A data inputs 8 through 15 to A0 through A7 in order.
   c. 1600A Q0 input to ROM 0 chip select line (1702A, pin 14). [3]
   d. 1600A clock input same as in Section 3.

[3]By qualifying on $\overline{CS}$ and triggering on A0 through A7, we derive a unique trigger that is effectively 12-bits wide with only the eight least significant bits displayed.

2. Connect 1607A data and clock inputs to microprocessor as follows:
   a. 1607A data inputs 0 through 3 to D0 through D3.
   b. 1607A data input 4 to CM-ROM.
   c. 1607A data input 5 to SYNC.
   d. 1607A clock input to $\phi 2$.
3. Set 1600A controls the same as in Section 4 with the following exceptions:

   Display Mode ..... Table A+B
   End Display ..... ON
   Delay ..... ON with Delay set to 8
   Qualifier ..... TRIG with Q0 set to LO
   Column Blanking ..... ccw
4. Set 1607A controls as follows:

   End Display ..... ON
   Delay ..... ON with Delay set to 8
   Logic [4] ..... NEG

[4]The microprocessor data bus uses negative logic, i.e., the most positive voltage is a logic "0" and the most negative voltage is a logic "1".

5. After a display is obtained, adjust 1607A column blanking to display 6 columns in Table B.

10. DISPLAY INTERPRETATION OF MULTIPLEXED DATA BUS

The state display photograph in figure 6 shows a comparison of the demultiplexed address and data buses (Table A) with the multiplexed microprocessor bus (Table B). Let's compare line 8 of Table A (trigger word) with the multiplexed data in Table B. Examination of the Sync line shows that line 6 of Table B corresponds with instruction cycle state A1. Note that the Sync and CM-ROM pulses are displayed as ones in the photograph since we have selected negative logic on the 1607A. Comparison of states A1, A2 and A3 (lines 6, 7, and 8 of the Table B state display) with the trigger word address bits reveal that the demultiplexer has correctly processed the address from the 4004. Similarly, comparison of trigger word data bits RD7 through RD0 with states M1 and M2 (lines 9 and 10 of the Table B display) shows that the multiplexer has correctly processed the ROM data onto the 4004 data bus. Note that the CM-ROM line is true during M2 state, indicating that the instruction being executed is an I/O instruction.

11. CONCLUSION

From the forgoing examples it may be concluded that efficient troubleshooting of the Intel 4004 Microprocessor system is expedited by two factors: first, the availability of the program listing as produced by 4004 cross assembler; and second, the availability of real time Logic State Analysis to display actual system operation for rapid error detection and correction.

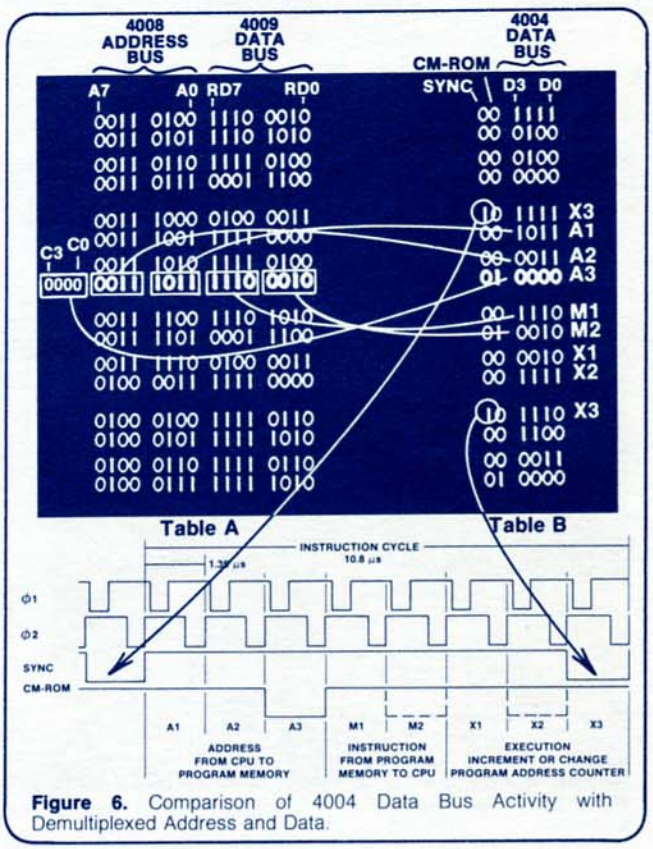


Figure 6. Comparison of 4004 Data Bus Activity with Demultiplexed Address and Data.

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Application Notes in the 167 series with the primary instrument(s) used in parenthesis.

167-1 The Logic Analyzer (5000A).
167-2 Digital Triggering for Analog Measurements (1601L).
167-3 Functional Digital Analysis (1601L).
167-4 Engineering in The Data Domain Calls for a New Kind of Digital Instrument (Describes measurement problems and various solutions with applicable instruments.)
167-5 Troubleshooting in the Data Domain is Simplified by Logic Analyzers (1600A and 1607A).
167-6 Mapping, a Dynamic Display of Digital System Operation (1600A).
167-7 Supplementary Data from Map Displays without Changing Probes (1600A).
167-8 Stable Displays of Disc System Waveforms Synchronized to Record Address (1620A).
167-9 Functional Analysis of Motorola M6800 Microprocessor Systems (1600A and 1607A).
167-10 Using the 1620A for Serial Pattern Recognition (1620A).
167-11 Functional Analysis of Intel 8008 Microprocessor Systems (1600A and 1607A).
167-12 Functional Analysis of Fairchild F8 Microprocessor Systems (1600A and 1607A).
167-13 The Role of Logic State Analyzers in Microprocessor Based Designs (1600A and 1607A).
167-14 Functional Analysis of 8080 Microprocessor Systems (1600A and 1607A).
167-15 Functional Analysis of Intel 4004 Microprocessor Systems (1600A and 1607A).
167-16 Functional Analysis of Intel 4040 Microprocessor Systems (1600A and 1607A).
167-17 Functional Analysis of National IMP Microprocessor Systems (1600A and 1607A).

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